REMARKS

Claims 1-8, 11-13, and 15-17 are presented for further examination. Claims 9, 10, and 14 have been canceled. Claims 1, 5, 7, 11, 12, 13, 15, 16, and 17 have been amended.

In the Office Action mailed June 30, 2004, the Examiner rejected claims 14-17 under 35 U.S.C. § 112, second paragraph, as indefinite because claim 14 included the limitation "the criteria" in line 2, which lacked antecedent basis. Claim 14 has been canceled, rendering this rejection moot.

Claims 1, 3-5, 7-10, and 13-14 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,940,618 ("Blandy et al."). Claims 2, 6, and 11-12 were found to be allowable if rewritten into independent form.

Applicants respectfully disagree with the basis for the rejection and request reconsideration and further examination of the claims.

The disclosed and claimed embodiments of the present invention incorporate two important steps and accompanying component structure that are not present in the Blandy et al. reference. More particularly, the method of evaluation and optimization of code utilizes a program counter trace that is converted into a format that defines a memory location associated with a function and an offset within the function. This format is illustrated, for example, in the right-hand column of Table 1 on page 7 of the specification, which is entitled "Annotated Trace Format." As described therein, the format is translated into physical addresses using a memory map to be evaluated, which is different from the memory map that is used to supply the first program counter trace.

Blandy et al., U.S. Patent No. 5,940,618, is directed to a system and method for monitoring performance in an information handling system that includes a collection phase, a placement phase, and an instrumentation phase. Blandy et al. teach a tracing program that collects instruction cache accesses and data cache accesses for the code segment to be monitored (see Blandy et al. at column 5, lines 22-24). As Blandy et al. state, this data collection step is highly intrusive. In addition, Blandy et al. teach a cache simulator that operates on this kind of trace data, cache geometry, and instrument code and data segments.

In contrast, the present invention is much simpler. It uses a model of a direct mapped cache and works on the physical addresses that have been translated from the program counter trace format. The cache simulator in Blandy et al. is complex, and it executes to determine a possible placement for the instrumentation code and data segments that will minimize cache mapping conflicts (see Blandy et al. at column 5, lines 58-60). In the present invention, the cache simulator merely receives physical addresses according to a map to be evaluated (converted from a program counter trace of a different map) and counts the total number of cache misses.

In the first Office Action, the Examiner asserts that Blandy et al. disclose the converting and translating steps. However, the part of Blandy et al. referenced by the Examiner in relation to the converting step (column 5, lines 21-28) refers to the tracing program that collects instruction cache accesses and data cache accesses. There is no disclosure in Blandy et al. of such a converting step.

The Examiner further suggests that the translating step is disclosed at column 5, lines 52-54. However, the only part the Examiner draws attention to is a reference to cache geometry of a directed map cache being supplied to a cache simulator. There is no reference in Blandy et al. to translating a trace format into physical addresses.

Turning to the claims, claim 1 is directed to a method of evaluating a set of memory maps for a program having a plurality of functions that includes the steps of executing a first version of the program according to a first memory map, to generate a program counter trace, converting the program counter trace into a program counter trace format defining a memory location in association with a function and an offset within the function using the first memory map; translating the program counter trace format into physical addresses using one of the set of memory maps to be evaluated, different from the first memory map; evaluating the number of likely cache misses by passing the physical addresses for that one memory map to a model of a direct-mapped cache; and repeating the previous two steps for each of the memory maps in the set. Claims 5, 7, and 13 have been similarly amended as claim 1 to include passing the physical addresses to a model of a direct-mapped cache or, in the case of claim 13, using the physical addresses for executing the translated trace on a cache model.

Nowhere do Blandy et al. teach or suggest the combination recited above, and in particular, the passing of the physical addresses for a memory map to a model of a direct-mapped cache. In view of the foregoing arguments, applicants respectfully submit that these claims, as well as all claims depending therefrom, are clearly in condition for allowance.

Claims 11, 12, 15, 16, and 17 have all been written into independent form to include limitations from dependent claims considered to be allowable by the Examiner. Applicants respectfully submit that these claims are also in condition for allowance.

In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Respectfully submitted,

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